Amendments to the Claims

A complete list of pending claims follows:

1. (Currently Amended) A computer system, comprising:

a processor;

a cache associated with the processor;

a system memory;

~~a write tracking buffer external to the processor, wherein the write tracking buffer is maintained in~~ a memory controller hub that is operable to track writes to the system memory by one or more bus masters operable to access the system memory;

a write tracking buffer external to the processor, wherein the write tracking buffer is communicatively coupled to the cache via the processor and to the system memory, and wherein the write tracking buffer is operable to hold as entries the addresses of one or more writes to the system memory made during [[the]] a period that the processor is in a low power state; [[and]]

wherein the memory controller hub is operable to:

initialize the write tracking buffer when the processor enters a low power state;

identify one or more writes to the system memory made during the period that the processor is in the low power state;

determine if the write tracking buffer is full during the period that the processor is in the low power state; and

if the write tracking buffer is not full, record the addresses of the one or more writes; and

wherein the processor is operable to write to the system memory one or more lines of cache prior to the processor entering its low power state, and wherein the processor is operable to invalidate [[the]] one or more lines of cache corresponding to the entries of the write tracking buffer upon the processor exiting its low power state.

2. (Currently Amended) The computer system of claim 1, wherein the low power state of the processor comprises a non-snoopable state in which the processor is not able to monitor accesses to the system memory.

3. (Previously Cancelled)

4. (Original) The computer system of claim 1, wherein the cache is an internal processor cache.

5. (Currently Amended) A method for managing the power consumption by a processor in a computer system, the computer system including a system memory and the processor including an internal cache, comprising the steps of:

maintaining a buffer in a memory controller hub that is operable to track one ore more writes to the system memory by one or more bus masters operable to access the system memory, wherein the buffer is:

external to the processor; and

communicatively coupled to the internal cache via the processor and to the system memory;

causing the processor to enter a low power state;

initializing the buffer when the processor enter the low power state;

during [[the]] a period that the processor is in a low power state[[,]]:

identifying one or more writes to the system memory made during the period;

determining if the buffer is full;

if the buffer is not full, recording one or more addresses ~~writing in a buffer external to the processor the addresses~~ of modified data in the system memory~~, wherein the buffer is maintained in a memory controller hub that is operable to track writes to system memory by bus masters operable to access system memory~~; and

upon the processor exiting the low power state, invalidating [[those]] one or more lines in the internal cache that correspond to the ~~memory~~ addresses recorded in the buffer.

6. (Original) The method for managing the power consumption by a processor in a computer system of claim 5, further comprising the step of invalidating the content of the buffer.

7. (Currently Amended) The method for managing the power consumption by a processor in a computer system of claim 5, wherein the step of causing the processor to enter a low power state comprises ~~the step of~~ causing the processor to enter a low power state in which the processor is unable to perform [[the]] a task of snooping accesses by the one or more bus masters to the system memory.

8. (Currently Amended) The method for managing the power consumption by a processor in a computer system of claim 5, wherein the step of writing to the buffer the addresses of modified data in the system memory comprises ~~the step of~~ writing to the buffer the address of each block of memory modified by [[a]] the one or more bus ~~master~~ masters of the computer system during the period that the processor is in the low power state.

9. (Currently Amended) The method for managing the power consumption by a processor in a computer system of claim 8, wherein the step of writing to the buffer the addresses of modified data in the system memory comprises ~~the step of~~ writing the address to the buffer only if it is determined that the address has not already been written to the buffer.

10. (Original) The method for managing the power consumption by a processor in a computer system of claim 9, further comprising the step of causing the processor to exit its low power state once the buffer is full.

11. (Currently Amended) The method for managing the power consumption by a processor in a computer system of claim 5, further comprising the step of, before causing the processor to enter the low power state, writing to the system memory the content of those lines of the internal cache that have been modified relative to the content [[of]] at the corresponding ~~locations~~ addresses in the system memory.

12. (Currently Amended) A method for managing cache coherency in an information handling system, the information handling system including a processor with an internal cache and a system memory, comprising the steps of:

maintaining a buffer in a memory controller hub that is operable to track one or more writes to the system memory by one or more bus masters operable to access the system memory, wherein the buffer is:

external to the processor; and

communicatively coupled to the internal cache via the processor and to the system memory;

performing a write back operation to write to the system memory [[those]] one or more cache lines that have been modified relative to [[the]] content [[of]] at corresponding memory ~~locations~~ addresses in the system memory;

causing the processor to enter a low power state;

initializing the buffer when the processor enter the low power state;

during [[the]] a period that the processor is in [[a]] the low power state[[,]]:

identifying one or more writes to system memory made during the period;

determining if the buffer is full;

if the buffer is not full, recording memory addresses ~~writing in a buffer external to the processor the addresses~~ of data in the system memory that have been modified by a bus master in the information handling system~~, wherein the buffer is maintained in a memory controller hub~~; and

upon the processor exiting the low power state for a higher power state, invalidating in the internal cache [[those]] one or more cache lines corresponding to the memory addresses recorded in the buffer.

13. (Original) The method for managing cache coherency in an information handling system of claim 12, further comprising the step of clearing the buffer following the step of invalidating the cache lines corresponding to the memory addresses recorded in the buffer.

14. (Currently Amended) The method for managing cache coherency in an information handling system of claim 12, further comprising the step of, following the step of invalidating cache lines corresponding to memory addresses recorded in the buffer, writing to the invalidated cache lines [[the]] content of [[the]] corresponding memory addresses in the system memory.

15. (Currently Amended) The method for managing cache coherency in an information handling system of claim 12, wherein the step of writing to the buffer comprises ~~the step of~~ writing to the buffer only if it is determined that the address of the modified memory location has not been previously recorded in the buffer.

16. (Original) The method for managing cache coherency in an information handling system of claim 12, further comprising the step of causing the processor to exit its low power state for a higher power state upon a determination that the buffer is full.

17. (Currently Amended) An information handling system, comprising:

a processor having an internal processor cache;

a system memory;

a buffer;

a memory controller;

wherein the memory controller is operable to populate the buffer with [[the]] one or more addresses of writes made to the system memory during [[the]] a period that the processor is in a low power state~~, and wherein the buffer is maintained in the memory controller~~;

wherein the buffer is:

maintained in the memory controller;

external to the processor; and

communicatively coupled to the internal processor cache via the processor and to the system memory;

wherein the memory controller is operable to:

initialize the buffer when the processor enters the low power state;

identify one or more writes to the system memory made during the period that the processor is in the low power state;

determine if the buffer is full during the period that the processor is in the low power state; and

if the buffer is not full, record the addresses of the one or more writes; and

wherein the processor, upon entering the low power state, is operable to write to the system memory one or more lines of cache and, upon exiting the low power state, is operable to invalidate cache lines of the internal processor cache corresponding to the addresses recorded in the buffer.

18. (Original) The information handling system of claim 17, wherein the low power state is a non-snoopable state characterized by the inability of the processor to monitor writes to system memory by a bus master of the information handling system.

19. (Original) The information handling system of claim 17, wherein the memory controller is operable to cause the processor to exit its low power state when the buffer is full.

20. (Currently Amended) The information handling system of claim 17, wherein the processor is operable to perform, before entering a low power state, a write-back operation to the system memory in which all modified cache lines are written to the corresponding locations in the system memory.

21. (Currently Amended) A method for managing cache coherency in a computer system following the entry of a processor into a low power state, the computer system including a processor having an internal cache, a system memory, and ~~an external~~ a write tracking buffer that

is external to the processor, is communicatively coupled to the internal cache via the processor and to the system memory, and is operable to store the addresses of system memory addresses modified during [[the]] a period that the processor was in the low power state, wherein the write tracking buffer is maintained in a memory controller hub that is operable to track one or more writes to the system memory by one or more bus masters operable to access the system memory, comprising the steps of:

causing the processor to enter a low power state;

initialize the write tracking buffer when the processor enter the low power state;

during the period that the processor is in a low power state:

identifying one or more writes to the system memory made during the period;

determining if the write tracking buffer is full;

if the write tracking buffer is not full, recording one or more memory addresses of modified data in the system memory;

causing the processor to exit the low power state; and

invalidating in the internal cache those cache lines corresponding to the one or more memory addresses stored in the write tracking buffer.

22. (Currently Amended) The method for managing cache coherency in a computer system of claim 21, further comprising the step of clearing the write tracking buffer following the step of invalidating cache lines in the internal cache.

23. (Currently Amended) The method for managing cache coherency in a computer system of claim 22, further comprising the step of, following the step of invalidating cache lines corresponding to memory addresses stored in the buffer, writing to the invalidated cache lines [[the]] content of the corresponding memory addresses in the system memory.